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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,673	PECHANEK ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-26 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on February 6th, 2006. The papers filed have been placed on record.

Specification

2. The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Election/Restrictions

1. Claims 1-26 are presented for examination.

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-8, drawn to a process and apparatus for partitioning a program into code segments, classified in class 712, subclass 205.

II. Claims 9-26, drawn to a processes and apparatus for expanding and condensing VLIW instructions, classified in class 712, subclass 24.

3. The inventions are distinct, each from the other because of the following reasons.

4. Inventions I and II are related as sub-combinations disclosed as usable together in a single combination. The sub-combinations are distinct from each other if they are shown to be separately usable. Invention I, a method and apparatus for partitioning code, is independently usable from VLIW instruction expansion and condensing,

wherein each invention can be used in separate systems that do not require the other. The VLIW instruction expansion and condensing in no way requires the invention of code partitioning, and vice versa. These inventions are distinctly different and would require a separate search and serious burden on the examiner. See MPEP § 806.05(d).

5. Because these inventions are distinct for the reasons given above and the search required for any one of group I and II is not required for any of the other groups, restriction for examination purposes as indicated is proper.

6. A telephone call was made to Joseph Agusta on April 10th, 2006 to request an oral election to the above restriction requirement, and Applicant elected invention II without traverse.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

8. Claims 1-8 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the telephonic interview with Joseph Agusta.

Claim Objections

9. Claims 9, 10, 11, 13, 15, 17, 18, 20, 21, 22, 23, 25 and 26 are objected to because of the following informalities: The use of the term "instruction slot" is unclear. Based on the claim language, it is impossible to tell if the instruction slot is referring to a particular memory location that contains a particular instruction, or perhaps some other intangible software code. Please amend the claims to clarify the situation to avoid a rejection under 35 USC 101. Appropriate correction is required.

10. Claim 17 is objected to because of the following informalities: The use of the acronyms are unclear, particularly as the acronym for very long instruction word, is abbreviated in later acronyms as just a 'V'. Perhaps a very long instruction memory basket should be abbreviated to VLIMB, rather than VIMB—and similarly for VIM and LIV. Additionally, spelling out the phrase in its entirety for each claim is also a viable option.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The word "basket" as disclosed is in claim 17 and would not be known to one of ordinary skill in the art. For the purpose of an art rejection for this

office action, a seemingly reasonable definition is used for the word "basket" in regards to computer architecture. See rejection of claim 17 below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371 (c) of this title before the invention thereof by the applicant for patent.

4. Claims 9, and 18-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Sheaffer (U.S. Patent No. 6,957,321).

5. Regarding claim 9, Sheaffer discloses a very long instruction word memory system (col 5 lines 48-51) comprising: a plurality of instruction slots for storing instruction words (col 7 lines 1-3); at least one of said plurality of instruction slots having an expanded format over the instruction format required in program storage for storing an expanded instruction having wider instruction width (col 1 lines 33-50 or col 2 line 65 to col 3 line 7);

Note that either method could be viewed as an expanded format.

And means for loading said at least one expanded format slot with an expanded instruction (col 7 lines 1-3).

Note the term "fetched" is considered to suggest loading an instruction.

6. Regarding claim 18, Sheaffer discloses a very long instruction word memory system (col 5 lines 48-51) comprising: a plurality of instructions in a native instruction format of a first bit width and format; and a very long instruction memory having slots for storing instructions of a second format having a second bit width and format different from that of the native instruction format (col 1 lines 33-50 or col 2 line 65 to col 3 line 7).

Note that in the first citation, the instruction with prefix and escape codes is considered to be the wide format. In the second citation, the instruction, with the additional NOP extensions, is considered to be the wide format. Although the prefix/escape codes are discussed in the background, they can be implemented with the present referenced invention, as indicated in col 7 lines 64-67.

7. Regarding claim 19, Sheaffer discloses the system of claim 18 wherein instructions are stored in a data memory and delivered to the very long instruction memory utilizing a data bus (col 5 lines 48-51 and col 7 lines 1-3 and fig 4 reference 410).

8. Regarding claim 20, Sheaffer discloses a very long instruction word memory system comprising: a plurality of instruction slots for storing instruction words (col 5 lines 48-51), at least one of said plurality of instruction slots having a compressed format with respect to an instruction format required in the program storage for storing a compressed instruction having narrower instruction width (col 1 lines 33-50 or col 2 line 65 to col 3 line 7);

Note that on paragraph 53 of Applicant's specification, the instructions designated as "compressed instructions" appear to be essentially the same as the extended instructions, just through a different view point. As claimed (in light of the Applicant's specification), it appears reasonable to consider the non-extended instruction a compressed instruction.

And means for loading said at least one compressed format slot with a compressed instruction (see below).

Note that the "compressed format" is considered to be a regular instruction without any escape bits, preflix bits, or NOP operands.

9. Regarding claim 21, Sheaffer discloses a processing apparatus comprising: a memory for storing a processing apparatus program comprising short instruction words (col 7 lines 1-3); an indirect very long instruction word (VLIW) memory comprising a plurality of instruction slots for storing instruction words (col 5 lines 48-51 and col 7 lines 1-3),

Note that the term "indirect" appears to be referring to an "indirect execution mechanism" in Applicant's specification. This mechanism is anticipated by the additional NOP operands that are indirectly used in execution.

At least one of said slot's instruction format sized according to execution function and operand storage capacity (col 3 lines 1-7)

Note that, clearly, the instruction slot is going to be sized based on the execution function (the size requirement for the execution units) and the operand storage capacity (the necessary bits required for the operand)

And independent of the short instruction word size (col 3 lines 1-7);

Note that the use of prefix/escape and NOP expansions indicates that the format is sized independent of the short instruction word size.

At least one data memory unit storing instruction operands (fig 4); and at least two execution units for executing the VLIW's instruction words (col 6 lines 35-36) in response to a short instruction word dispatched from the memory (see below).

Note that the VLIW instruction is comprised of several short instruction words, indicating that the execution units will execute the VLIW instruction words in response to a short instruction word.

10. Regarding claim 22, Sheaffer discloses the processing apparatus of claim 21 wherein the short instruction words comprise K-bits (fig 5) and the slot's instruction format comprises T-bits, wherein T.noteq.K (col 3 lines 1-7).

Note that the short instruction words have a different number of bits than the instruction slot, the slot considered to hold the additional bits in the extensions for either escape/prefix codes or NOP operands.

11. Regarding claim 23, Sheaffer discloses the processing apparatus of claim 22 wherein the slot's instruction format comprises at least one operand address field of B-bits supporting direct operand addressing (fig 4a reference 515).

12. Regarding claim 24, Sheaffer discloses the processing apparatus of claim 23 wherein the data memory unit has a capacity 2.sup.B data values (see below).

Note that it is clearly implied that there are 2^B data values. That is the whole point of having B bits in an address.

13. Regarding claim 25, Sheaffer discloses the processing apparatus of claim 21 wherein the at least one of the two execution units operate on a slot instruction format and directly access operands from the data memory unit for execution (fig 5 and col 3 lines 1-7).

Note that the instructions do not necessarily have to contain any extensions. They can just be regular instructions. Consequently, the execution units can directly access operands from the data memory unit for execution. Additionally, as shown in fig 5, some operands are accessed directly even when an NOP instruction extension takes place.

14. Regarding claim 26, Sheaffer discloses the processing apparatus of claim 21 wherein the two execution units operate as one execution unit (col 6 lines 35-36)

Note that it is unclear how two execution units can operate as one execution unit. For the purpose of this office action, the two execution units execute mutually exclusive instructions and do not replicate any work done by another execution unit; this is considered to be working as one execution unit.

When executing two VLIW memory slot instructions as specified by a two slot XV indirect VLIW instruction (fig 5 and col 5 lines 49-51),

Note that an XV instruction (which appears to be an execute VLIW instruction in Applicant's specification) is considered to be a VLIW instruction executed in the processor or, essentially, a typical VLIW instruction.

And wherein the two execution units operate as one execution unit when executing one VLIW memory slot instruction as specified by a one slot XV indirect VLIW instruction (col 3 lines 1-7).

Note that VLIW instructions can take up a varying number of slots, depending on how the compiler combines the short instructions into VLIW instructions. Consequently, the execution unit executes the VLIW instructions no matter what number of "slots" are occupied by this instruction.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 10, 11, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer in view of Moller (U.S. Patent No. 6,826,522).

17. Regarding claim 10, Sheaffer discloses the memory system of claim 9 wherein the plurality of instruction slots comprise a store unit instruction slot (col 9 lines 13-19), a load unit instruction slot (col 9 lines 13-19),

Note that the storing of instructions clearly implies the necessity of a loading unit as well, otherwise the stored instructions could not be accessed and no interesting program would be able to run on this processing unit.

An arithmetic logic unit (ALU) instruction slot (col 9 lines 14-15), and a data store unit (DSU) instruction slot (col 9 lines 13-19).

Sheaffer fails to disclose a multiply accumulate unit instruction slot.

Moller discloses a multiply accumulate instruction unit (col 5 lines 11-12)

Sheaffer, a computer system that already contains an arithmetic logic unit, would likely be motivated to include instructions that provide further flexibility to the programmer. A multiply accumulate instruction is well known in the art and allows the programmer to complete varies applications in one instruction, rather than two—making

the system less complicated and often faster. For these reasons, Sheaffer would be motivated to include a multiply accumulate instruction.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the computing system of Sheaffer and include the multiply accumulate instruction/unit of Moller. Clearly, as this instruction is incorporated, instruction slots would be available to save a MAC instruction in instruction memory.

18. Regarding claim 11, Sheaffer discloses the memory system of claim 10 wherein the store unit instruction slots store expanded store instructions including additional bits to extend compute register file addressing, an additional bit to extend address register file addressing (col 3 lines 16-19), an additional bit to expand an opcode file, or an additional bit to extend a conditional field.

Note that the "or clause" of the claim requires only one limitation to be anticipated.

19. Regarding claim 13, Sheaffer discloses the memory system of claim 10 where the load unit instruction slots store expanded load instructions of a first format for load immediate operations including additional bits to extend compute register file addressing, a bit to extend address file register addressing (col 3 lines 16-19 and col 9 lines 13-19),

Note, in the second citation, that the result is stored in a double-wide register. Since this is treated as one register, this would suggest that loading would work the same way, extending the register addressing.

A bit to extend a conditional field or sixteen bits to extend an immediate field.

Note that, again, the "or clause" of the claim requires only one limitation to be anticipated.

20. Regarding claim 15, Sheaffer discloses the memory system of claim 10 where the ALU, MAU and DSU instruction slots store expanded instructions including additional bits in each operand field to extend compute register file addressing (col 9 lines 13-19), a bit to extend an opcode field, or a bit to extend a data type field.

21. Claims 12, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer/Moller in view of Tremblay (U.S. Patent No. 6,341,348).

22. Regarding claim 12, Sheaffer discloses the memory system of claim 11. wherein said extended instructions support expansion of a 32.times.32 bit/16.times.64 bit configurable register file (103 with Tremblay) size to a 128.times.32 bit/64.times.64 bit/32.times.128 bit configurable register file size.

Sheaffer/Moller fails to disclose a register file of size 128.times.32 bit/64.times.64 bit/32.times128 bit.

Tremblay discloses a register file with 128 32-bit registers (col 5 lines 39-41).

Sheaffer/ Moller fails to disclose the size of its register file. Sheaffer/Moller would likely be motivated to utilize a similar size as another VLIW invention (Tremblay col 5 line 57). Clearly, the size of the register file depends on particular aspects of the invention not necessarily disclosed in a patent attributed to a specific feature. Sheaffer/Moller would have been reasonably motivated to utilize a register file of any reasonable size.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the invention of Sheaffer/Moller and incorporate a register file with 128 32-bit registers. Sheaffer also discloses the technique of grouping registers into pairs and quads (col 1 line 66 to col 2 line 8), allowing for a register file with 64 64 bit registers and 32 128 bit registers.

Note that it is unclear how the claimed register file is being expanded. This claim appears to be simply claiming a register file of the larger size given.

23. Regarding claim 14, Sheaffer discloses the memory system of claim 13 wherein said extended instructions support expansion of a 32.times.32 bit/16.times.64 bit configurable register file size to a 128.times.32 bit/64.times.64 bit/32.times.128 bit configurable register file size (Tremblay col 5 lines 39-41 and Sheaffer col 1 line 66 to col 2 line 7--see claim 12).

24.

Regarding claim 16, Sheaffer discloses the memory system of claim 15 wherein said extended instructions support expansion of a 32.times.32 bit/16.times.64 bit configurable register file size to a 128.times.32 bit/64.times.64 bit/32.times.128 bit configurable register file size (Tremblay col 5 lines 39-41 and Sheaffer col 1 line 66 to col 2 line 7--see claim 12).

25. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer in view of Oinaga (U.S. Patent No. 4,665,479).

26. Regarding claim 17, Sheaffer discloses a very long instruction word (VLIW) instruction (col 5 lines 48-51) memory (VIM) basket (VIMB) (col 7 lines 1-3)

Note that it is unclear what is meant by the term "memory basket". A basket is a device used to place items for later use, so a VLIW basket would appear to be a place to store VLIW instructions, namely an instruction memory.

an instruction bit organizer for receiving instructions as data and organizing the bits from the data encoded instructions into proper format for loading into the VIMB (see below);

Note that instruction memory requires some sort of logic, namely a memory controller. This memory controller is considered to be an instruction bit organizer. This Instruction bit organizer will clearly take the data encoded instructions and put them in proper order for loading into the instruction memory (VIMB).

And the VIMB comprising a plurality of instruction slots having expanded instruction slot width greater than the width of the instruction format required in program storage (col 1 lines 33-50 or col 2 line 65 to col 3 line 7).

Sheaffer fails to disclose a load indirect instruction or a mask bit field specifying which slots will be loaded.

Oinaga discloses a load indirect instruction (col 2 lines 9-14) and a load mask bit field (col 4 lines 53-57).

The use of load indirect instructions are commonly used in the art. They exist to give an instruction the ability to load all addressable sections of memory with the minimum amount of bits necessary, a technique that saves both time and space, clear motivation for Sheaffer. Additionally, a load mask bit field is also commonly used in the art. This technique allows for certain loaded bits to be masked, loading only portions of a register rather than the entire register. This allows for flexibility for certain applications that would be far more complicated without this feature—again, clear motivation for Sheaffer.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the processing system of Sheaffer to include a load indirect instruction and masking mechanism, as in Oinaga.

Conclusion

27. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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